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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,955	01/30/2004	Hiroyuki Yamashita	1687.1005	2505

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,955	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/766,955 filed 01/20/2003.

2. Claims 1- 7 are pending in the Application.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 4-7 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Semeria et al. ("Methodology for hardware/software co-verification in C/C++", 25-28 Jan. 2000).

With respect to claim 1 Semeria et al. teaches a method for co-verifying hardware and software, by using a host CPU, for a semiconductor device on which at least one target CPU and one OS are mounted within a method of hardware/software

co0verification with simulation of a processor model, wherein verification is for testing of system-on-chip (Page 405, left column; abstract) and software runs on the host processor (Page 406, left column), the hardware/software co-verification method comprising the steps of: (a) inputting, as a verification model, a timed software component described in a C-based language and compiling the same by using C/C++ based design environment for describing software to model all parts of the system (abstract), wherein SystemC environment is used including supporting operating system (OS) (Page 406, left column) and ISS (instruction set simulator) is integrated with BFM (bus functional model) for timing accurate simulation of the IC (Page 407, left column), inputting as a verification model a hardware component described in the C-based language and compiling the same within C/C++ based design environment by describing the hardware in C/C++ language (abstract, and linking together the compiled timed software component and the compiled hardware component within a designer choice of making the software described in C/C++ language execute in parallel with the hardware described in C/C++ language (Page 407, left column), wherein compilation of the program written in C/C++ is processed very efficiently (Page 408, right column); (b) inputting a testbench and compiling the same by reusing the testbench that were developed during system validation (Page 405, left column); (c) linking together the verification models processed in step (a) and the testbench processed in step (b) as shown in the example of testing the hardware dw8051illustrated by Table 1, wherein the hardware model, software model and testbench are linked together in the file written in C++ language (Page 408, left column); (d) performing a simulation based on an

executing program generated in step (c) (abstract); and (e) outputting a result of the simulation performed in step (d) within providing detailed report at the end of the simulation by performing estimation functions (Page 406, right column) wherein several techniques for improving simulation speed is used (Page 407, right column).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Semeria et al. as applied to claim 1 above, and further in view of Bade et al. (US Patent Application Publication 2002/0059054).

With respect to claim 2 Semeria et al. teaches a method for co-verifying hardware and software, by using a host CPU, for a semiconductor device on which at

least one target CPU and one OS are mounted within a method of hardware/software co0verification with simulation of a processor model, wherein verification is for testing of system-on-chip (Page 405, left column; abstract) and software runs on the host processor (Page 406, left column), the hardware/software co-verification method comprising the steps of: (a) inputting as a verification model, a timed software component constructed from binary code native to the host CPU by using C/C++ based design environment for describing software to model all parts of the system (abstract), wherein SystemC environment is used including supporting operating system (OS) (Page 406, left column) and ISS (instruction set simulator) is integrated with BFM (bus functional model) for timing accurate simulation of the IC (Page 407, left column), inputting as a verification model a hardware component described in a C-based language and compiling the same, and linking together the input timed software component and the compiled hardware component within C/C++ based design environment by describing the hardware in C/C++ language (abstract, and linking together the compiled timed software component and the compiled hardware component within a designer choice of making the software described in C/C++ language execute in parallel with the hardware described in C/C++ language (Page 407, left column), wherein compilation of the program written in C/C++ is processed very efficiently (Page 408, right column); (b) inputting a testbench and compiling the same by reusing the testbench that were developed during system validation (Page 405, left column); (c) linking together the verification models processed in step (a) and the testbench processed in step (b) as shown in the example of testing the hardware

dw8051illustrated by Table 1, wherein the hardware model, software model and testbench are linked together in the file written in C++ language (Page 408, left column); (d) performing a simulation based on an executing program generated in step (c) (abstract); and (e) outputting a result of the simulation performed in step (d) within providing detailed report at the end of the simulation by performing estimation functions (Page 406, right column) wherein several techniques for improving simulation speed is used (Page 407, right column). However Semeria et al. lacks the specifics regarding construction of the software component from binary code native. Bade et al. teaches computer-aided system for improving the evaluation of the IC design including virtual embedded systems (abstract), designing hardware portion and software portion (paragraph [0007], integrating them before the simulation process (paragraph [0104], wherein the software debugger is adapted to permit at least one binary code of a software application compiled for a target processor (hardware) (paragraph [0021]). It would have been obvious to one of ordinary skill in art at the time the invention was made to have used Bade et al. to teach the specifics subject matter Semeria et al. does not teach, because the virtual embedded system has an execution speed sufficiently high to permit the evaluation benchmark software executing on the virtual embedded system (paragraph [0021]).

With respect to claim 3 Semeria et al. teaches a method for co-verifying hardware and software, by using a host CPU, for a semiconductor device on which at least one target CPU and one OS are mounted within a method of hardware/software co0verification with simulation of a processor model, wherein verification is for testing of

system-on-chip (Page 405, left column; abstract) and software runs on the host processor (Page 406, left column), the hardware/software co-verification method comprising the steps of: (a) inputting as a verification model a timed software component described in a C-based language and compiling the same by using C/C++ based design environment for describing software to model all parts of the system (abstract), wherein SystemC environment is used including supporting operating system (OS) (Page 406, left column) and ISS (instruction set simulator) is integrated with BFM (bus functional model) for timing accurate simulation of the IC (Page 407, left column), inputting as a verification model a timed software component constructed from binary code native to the host CPU and compiling the same, inputting as a verification model a hardware component described in the C-based language and compiling the same, and linking together the compiled or input timed software components and the compiled hardware component within C/C++ based design environment by describing the hardware in C/C++ language (abstract, and linking together the compiled timed software component and the compiled hardware component within a designer choice of making the software described in C/C++ language execute in parallel with the hardware described in C/C++ language (Page 407, left column), wherein compilation of the program written in C/C++ is processed very efficiently (Page 408, right column); (b) inputting a testbench and compiling the same by reusing the testbench that were developed during system validation (Page 405, left column); (c) linking together the verification models processed in step (a) and the testbench processed in step (b) as shown in the example of testing the hardware dw8051illustrated by Table 1, wherein

the hardware model, software model and testbench are linked together in the file written in C++ language (Page 408, left column); (d) performing a simulation based on an executing program generated in step (c) (abstract); and (e) outputting a result of the simulation performed in step (d) within providing detailed report at the end of the simulation by performing estimation functions (Page 406, right column) wherein several techniques for improving simulation speed is used (Page 407, right column). However Semeria et al. lacks the specifics regarding construction of the software component from binary code native. Bade et al. teaches computer-aided system for improving the evaluation of the IC design including virtual embedded systems (abstract), designing hardware portion and software portion (paragraph [0007], integrating them before the simulation process (paragraph [0104], wherein the software debugger is adapted to permit at least one binary code of a software application compiled for a target processor (hardware) (paragraph [0021]). It would have been obvious to one of ordinary skill in art at the time the invention was made to have used Bade et al. to teach the specifics subject matter Semeria et al. does not teach, because the virtual embedded system has an execution speed sufficiently high to permit the evaluation benchmark software executing on the virtual embedded system (paragraph [0021]).

With respect to claims 4-7 Semeria et al. teaches:

Claims 4 and 6: in order to generate in advance the timed software component described in the C-based language from an untimed software component described in ANSI-C, the method further comprises the steps of: inputting the untimed software component described in ANSI-C within BFM abstract processor model, which provides

programming interface that can be used by the software directly, wherein this model is untimed (Page 406, left column), and recognizing basic blocks and inserting control points within interrupt controller implemented as a part of BFM (Page 406, right column); generating binary code native to a target CPU by compiling the untimed software component in which the control points have been inserted by using BFM for co-simulation at early stage of the design process as shown on the Fig. 1a, and since it's written in C++ language outputting the binary code native to a target CPU (Page 406, left column); computing execution time between the control points in the generated binary code native to the target CPU within detecting the interrupts by interrupt controller , which gives an opportunity to execute a user defined function (Page 406, right column); and inserting, in accordance with the computed execution time, an execution time insertion statement at each of the control points inserted in the untimed software component, and thus outputting the timed software component described in the C-based language within integrating ISS and BFM to perform detailed cycle accurate simulation (Page 406, left column), wherein the instruction set simulator is used and ISS software will register internal ISS routines as handlers for the interrupts (Page 406, right column; Page 407, left column);

Claims 5 and 7: in order to generate in advance the timed software component constructed from the binary code native to the host CPU from an untimed software component constructed from binary code native to a target CPU, the method further comprises the steps of: inputting the untimed software component constructed from the binary code native to the target CPU within BFM abstract processor model, which

provides programming interface that can be used by the software directly, wherein this model is untimed (Page 406, left column), and converting the same into a software component expressed in the binary code native to the host CPU by compiling the untimed software component in which the control points have been inserted by using BFM for co-simulation at early stage of the design process as shown on the Fig. 1a, and since it's written in C++ language outputting the binary code native to a target CPU (Page 406, left column); recognizing basic blocks and inserting control points in the software component expressed in the binary code native to the host CPU within interrupt controller implemented as a part of BFM (Page 406, right column); computing execution time between the control points in the software component in which the control points have been inserted within detecting the interrupts by interrupt controller , which gives an opportunity to execute a user defined function (Page 406, right column); and inserting, in accordance with the computed execution time, binary code functionally equivalent to an execution time insertion statement at each of the control points inserted in the software component, and thus outputting the timed software component constructed from the binary code native to the host CPU within integrating ISS and BFM to perform detailed cycle accurate simulation (Page 406, left column), wherein the instruction set simulator is used and ISS software will register internal ISS routines as handlers for the interrupts (Page 406, right column; Page 407, left column).

However Semeria et al. lacks the specifics regarding construction of the software component from binary code native. Bade et al. teaches computer-aided system for improving the evaluation of the IC design including virtual embedded systems

(abstract), designing hardware portion and software portion (paragraph [0007], integrating them before the simulation process (paragraph [0104], wherein the software debugger is adapted to permit at least one binary code of a software application compiled for a target processor (hardware) (paragraph [0021]). It would have been obvious to one of ordinary skill in art at the time the invention was made to have used Bade et al. to teach the specifics subject matter Semeria et al. does not teach, because the virtual embedded system has an execution speed sufficiently high to permit the evaluation benchmark software executing on the virtual embedded system (paragraph [0021]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

STACY A. WHITMORE
PRIMARY EXAMINER